Switched-Mode High-Efficiency Microwave Power Amplifiers in a Free-Space Power-Combiner Array

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***Abstract*— A design-oriented analysis of the microwave transmission-line class-E amplifier is presented. Experiments and harmonic-balance circuit simulations verify the theoretical equations which predict class-E-amplifier output power, maximum frequency of operation, and dc–RF conversion efficiency. Experimental results at 0.5, 1, 2, and 5 GHz are presented. At 0.5 GHz, 83% drain efficiency and 80% power-added efficiency (PAE) are measured, with an output power of 0.55 W, using the Siemens CLY5 MESFET. These results are compared to a class-A and class-F power amplifier using the same device. At 5 GHz, 81% drain efficiency and 72% PAE are measured, with an output power of 0.61 W, using the Fujitsu FLK052WG MESFET. Finally, the 5-GHz class-E power amplifier is successfully integrated into an active-antenna array, demonstrating power combining of four elements with an 85% power-combining efficiency. At 5.05 GHz, the class-E power-amplifier antenna array delivers a total of 2.4 W of output power, with a dc–RF conversion efficiency of 74% and a PAE of 64%.**

***Index Terms*— Free-space power combining, high-efficiency amplifiers, power-added efficiency.**

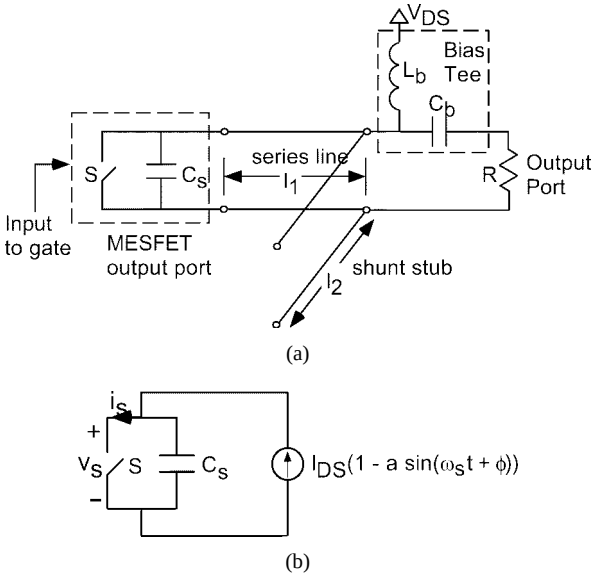

Fig. 1. (a) The transmission-line class-E high-efficiency circuit. (b) The class-E circuit assuming sinusoidal load current.

I. Introduction

ACHIEVING high efficiency in microwave amplifiers is important for reducing the size and weight, and increasing the output power, battery lifetime, and reliability of portable wireless transmitters. By increasing the efficiency of an amplifier from 50% to 90%, the dissipated heat power is reduced by a factor of nine for the same output power. Currently, microwave amplifiers have demonstrated 72% power-added efficiency (PAE) with 1 W of output power at 12 GHz [1], 47% PAE with 0.5 W of output power at 20 GHz [2], and 29% PAE with 1 W of output power at 40 GHz [3]. The goal of this paper is to take advantage of rapid improvements in device technology, enabling design and analysis of very high-efficiency switched-mode power amplifiers.

The idea of harmonically tuning RF power amplifiers has existed since at least 1958 [4] and 1967 [5]. In both [4] and [5], a short circuit is presented to the output of the transistor (or vacuum tube) at even harmonics, and an open circuit is presented at all of the odd harmonic frequencies. In [6], Raab coins the term "class F" for this type of harmonically tuned amplifier operation. Since the 1980's, numerous researchers have successfully applied the class-F concept to microwave solid-state power amplifiers [7]–[9].

The class-E amplifier, invented in 1975 by the Sokals [10], is particularly promising for high-frequency high-efficiency power generation. In [11], Raab first makes the assumption of sinusoidal current flow in the output of the class-E circuit used in this paper. Fig. 1(a) shows the class-E switched-mode amplifier topology. The active device (in this case a MESFET) acts as a switch, and the circuit must be properly designed to give class-E operation. At low RF frequencies, such circuits have demonstrated efficiencies as high as 96% [10]. However, at microwave frequencies, transistors are not ideal switches due to parasitic device capacitances. These parasitics can be

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deembedded from the device and included in the tuned circuit design [12]. The capacitance C_s in the circuit in Fig. 1(a) is the intrinsic output capacitance of the transistor, while the lead inductance of the device may be accounted for by shortening the series transmission line l_1. The efficiency is limited primarily by the drain-to-source saturation resistance of the transistor and the lossy properties of its parasitic elements. It is shown here that even in a degraded class-E mode, high efficiency and power can still be achieved.

Recently, the transmission-line class-E amplifier has been experimentally demonstrated at 0.5, 1, and 2 GHz [12]. In this paper, a design-oriented analysis of the transmission-line class-E amplifier is presented and experimental results are extended to 5 GHz. Harmonic-balance circuit simulations verify that the amplifiers operate in class-E mode. Finally, the 5-GHz class-E transmission-line amplifier is integrated into an active-antenna power-combining array.

II. Design-Oriented Analysis of Class-E Amplifiers

A. Assumptions Made in the Analysis

There are several assumptions made in the simplified analysis of the class-E circuit presented here [see Fig. 1(a)].

1) A 50% duty cycle is used. This is shown in [11] to be the optimal case.
2) The switching device has zero on-resistance and infinite off-resistance.
3) The shunt capacitor C_s is the output capacitance of the transistor and is assumed to be linear in the initial analysis.
4) L_b acts as an ideal bias choke (open circuit at RF).
5) There are no losses in the circuit shown in Fig. 1(a), except into the load R. Therefore, all of the dc power $V_{\rm DS}I_{\rm DS}$ is dissipated in R (100% efficiency operation).
6) The external load network has a high Q-factor and constrains the current flowing into it to be approximately sinusoidal at the switching frequency.

These assumptions significantly simplify the basic explanation of the class-E circuit, and allow tractable equations to describe its operation [11]. The exact time-domain solution of the class-E switched-mode circuit involves a set of differential equations, which give little insight into the basic tradeoffs of the circuit, are tedious to solve, and are not useful for design [13].

B. Switch Voltage and Current Waveforms

The assumptions used in this analysis are illustrated in Fig. 1(b). An equivalent current source, which consists of a constant (dc) and sinusoidal (RF) component, is placed across the switched capacitor. The class-E amplifier is thus reduced to a simple first-order circuit.

It is seen in Fig. 1(b), when the switch is turned ON, that there is no voltage across the switch, but a piece of sinusoidal current (with a dc component) flows through it. When the switch is turned OFF, the sinusoidal current continues to flow, but now it flows through the shunt capacitive part of the switch.

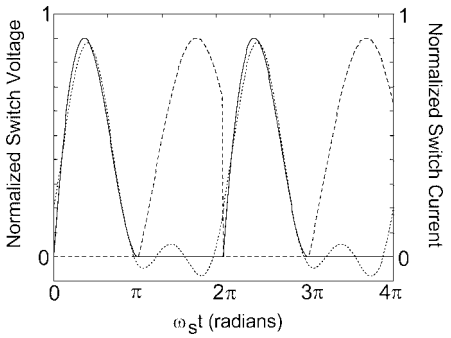

Fig. 2. The switch-voltage waveform with two harmonics taken into account (dotted line), plotted along with the ideal class-E switch-voltage waveform (solid line) and ideal current waveform (dashed line).

During the OFF interval,

$$v_s(t) = \frac{1}{C_s}\int_0^t I_{\rm DS}(1 - a\sin(\omega_s t' + \phi))\,dt'. \qquad (1)$$

The integral implicitly assumes that $v_s(0) = 0$, which is one of the three boundary conditions imposed upon $v_s(t)$ by definition of class E. Thus,

$$v_s(t) = \frac{I_{\rm DS}}{\omega_s C_s}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)). \qquad (2)$$

The other two conditions for class-E operation are $v_s(T_s/2) = 0$ and $\mathrm{d}v_s/\mathrm{d}t(T_s/2) = 0$. The first condition avoids shorting the capacitor C_s when there is voltage across it during switching, and the second condition ensures a "soft" turn-on condition for the switching device. The two additional constraints determine a and ϕ uniquely

$$a = \sqrt{1 + \frac{\pi^2}{4}} \simeq 1.862 \qquad (3)$$

$$\phi = -\arctan\frac{2}{\pi} \simeq -32.48^\circ \qquad (4)$$

where a and ϕ are constants for *any* high-Q class-E circuit with a capacitor in shunt with the switch and a 50% duty cycle. Now the voltage and current across the switch are known and are plotted in Fig. 2.

C. Relationship Between $V_{\rm DS}$ and $I_{\rm DS}$

It is of interest to find the relationship between $V_{\rm DS}$ and $I_{\rm DS}$, or in other words, how much current is drawn for a given supply voltage or vice-versa. $V_{\rm DS}$ is the dc component of $v_s(t)$, the voltage across the switch. Taking the time average of the switch voltage over the period gives $V_{\rm DS} = I_{\rm DS}/\pi\omega_s C_s$, thus, the dc power is given by

$$P_{dc} = I_{\rm DS}V_{\rm DS} = \pi\omega_s C_s V_{\rm DS}^2. \qquad (5)$$

This simple result has important implications for a practical microwave class-E circuit, assuming that the minimum value of C_s is the parasitic capacitance of a microwave device, e.g., $C_{\rm ds}$ of a MESFET. At a specified frequency, a device with an output capacitance C_s must operate at some supply voltage $V_{\rm DS}$. Since ω_s, C_s, and $V_{\rm DS}$ are now specified, the device must be able to handle the required maximum current, which is $(1 + a)I_{\rm DS} \simeq 2.86I_{\rm DS}$. Due to this transistor limitation, an

approximate maximum frequency of class-E operation can be found for a given device

$$f_{\max} = \frac{I_{\rm DS}}{2\pi^2 C_s V_{\rm DS}} = \frac{I_{\max}}{C_s V_{\rm DS}} \frac{1}{2\pi^2(1+a)} \simeq \frac{I_{\max}}{56.5 C_s V_{\rm DS}}. \quad (6)$$

For higher drain-bias voltages, the maximum frequency of operation decreases. For example, the Siemens CLY5 MESFET considered in Section II-D has $I_{\max} \simeq 1200$ mA and $C_s \simeq 2.6$ pF. For this transistor at a dc drain voltage of $V_{\rm DS} = 6$ V, $f_{\max} \simeq 1.4$ GHz. Above these frequencies, this device cannot be used for an *ideal* class-E circuit, although an approximation to class-E operation may be obtained at higher frequencies with some degradation in maximum achievable efficiency [14].

D. Fundamental-Frequency Class-E Load Impedance

Finding the dc component of $v_s(t)$ yields an expression relating the dc parameters of the class-E circuit ($V_{\rm DS}$ and $I_{\rm DS}$). Finding the fundamental-frequency component of $v_s(t)$ yields information about the RF impedances in the circuit. The fundamental component of current flowing into the load network $i_{\rm net_1}$ was found above (its magnitude is $aI_{\rm DS}$ and its phase is ϕ). However, the fundamental component of the load voltage v_{s_1} must be found using Fourier-series expansions. Only the following results are presented here:

$$v_{s_1} = a_0 I_{\rm DS} \sin(\omega_s t + \phi_0) \quad (7)$$

$$i_{\rm net_1} = a I_{\rm DS} \sin(\omega_s t + \phi) \quad (8)$$

where the constants a_0 and ϕ_0 are given by

$$a_0 = \frac{1}{\omega_s C_s} \sqrt{\frac{\pi^2}{16} + \frac{4}{\pi^2} - \frac{3}{4}} \quad (9)$$

$$\phi_0 = \frac{\pi}{2} + \arctan\left(\frac{2\pi}{8-\pi^2}\right) \quad (10)$$

and a and ϕ are given in (3) and (4). The following phasor impedance of the external load network can now be found:

$$Z_{\rm net_1} = \frac{a_0}{a} e^{j(\phi_0 - \phi)} = \frac{\kappa_0}{\omega_s C_s} e^{j\theta_0} \simeq \frac{0.28015}{\omega_s C_s} e^{j49.0524^\circ}. \quad (11)$$

The required load angle for class-E operation with a capacitor in shunt with the switch is a constant. To ensure class-E operation, all that is needed is a specific fundamental impedance of $Z_{\rm net_1}$, and open-circuit conditions at all of the higher harmonic frequencies. Applying standard transmission-line formulas to the transmission-line-load network topology [shown in Fig. 1(a)], two equations are found relating the transmission-line lengths and characteristic admittances to produce the desired fundamental impedance condition [12]. The electrical lengths of lines l_1 and l_2 should be close to 45°, so that an approximate open circuit will be presented to the switched capacitor at the second harmonic. The characteristic impedances of the lines may be adjusted to enforce this condition. Additional methods of enforcing harmonic open circuit conditions are described in [13]. For a packaged device, the lead inductance connecting the switched capacitor to the series transmission line l_1 is significant; this is accounted for by shortening the length of l_1.

E. Fourier Series of Switch Voltage

The simplified analysis of the class-E circuit given above assumes a sinusoidal output signal at the load resistor R. In practice, some residual higher harmonic components will be present at the output of the circuit, depending upon the particular choice of load network topology and specific design values for the elements. In this section, the switch voltage $v_s(t)$ found above is analyzed using the Fourier series, and expressions for the magnitude and phase of the harmonics of switch voltage are given. These general results can then be transformed through any specific load network to find explicit expressions for the harmonic content at the output of the class-E amplifier. Furthermore, it is shown that a good approximation to class-E operation may be obtained with only two harmonics of the switch-voltage waveform.

An expression for switch voltage $v_s(t)$ was derived in (2)–(4). The Fourier series is defined as

$$v_s(t) = \sum_{n=-\infty}^{\infty} K_n e^{jn\omega_s t} \quad (12)$$

$$K_n = \frac{I_{\rm DS}}{2\pi\omega_s C_s} \int_0^{\pi} ((\omega_s t) + a(\cos((\omega_s t) + \phi) - \cos\phi) \cdot e^{-jn(\omega_s t)} d(\omega_s t). \quad (13)$$

The integration is performed only over the first half of the period, when $v_s(t)$ is nonzero, and $(\omega_s t)$ is used as the integration variable. The results are

$$v_{sn}(t) = a_n I_{\rm DS} \sin(n\omega_s t + \phi_n) \quad (14)$$

$$a_n = \frac{2|K_n|}{I_{\rm DS}}$$

$$\phi_n = \frac{\pi}{2} + \angle K_n \quad (15)$$

$$(n \text{ odd } n \neq 1)\text{: } K_n = \frac{I_{\rm DS}}{\pi\omega_s C_s}\left(-\frac{1}{n^2}\right) \quad (16)$$

$$(n \text{ even, } n \neq 0)\text{: } K_n = \frac{I_{\rm DS}}{\pi\omega_s C_s}\left(\frac{2n + j\pi}{2n(1-n^2)}\right) \quad (17)$$

$$(n = 1)\text{: } K_1 = \frac{I_{DS}}{\pi\omega_s C_s}\left(\frac{\pi^2}{8} - 1 - \frac{j\pi}{4}\right). \quad (18)$$

These expressions may be used to find the magnitude and phase of any number of harmonics of the ideal class-E switch-voltage waveform. In Fig. 2, for example, the first two harmonics of the switch-voltage waveform are plotted along with the ideal waveforms. Two harmonics of the switch voltage adequately represent the salient form of class-E operation.

F. Efficiency Analysis

For microwave class-E amplifiers using low-loss reactive elements (such as microstrip transmission lines), the majority of loss occurs within the transistor. During the OFF-state, the transistor looks primarily reactive (the intrinsic device looks like a capacitor at its output port), and during the ON-state, the transistor looks like a small resistor. It is the ON-state resistance which may be estimated from the MESFET's I–V curves, which is primarily responsible for its lossy behavior. The transistor-output port model used here is modified from the model proposed in [15].

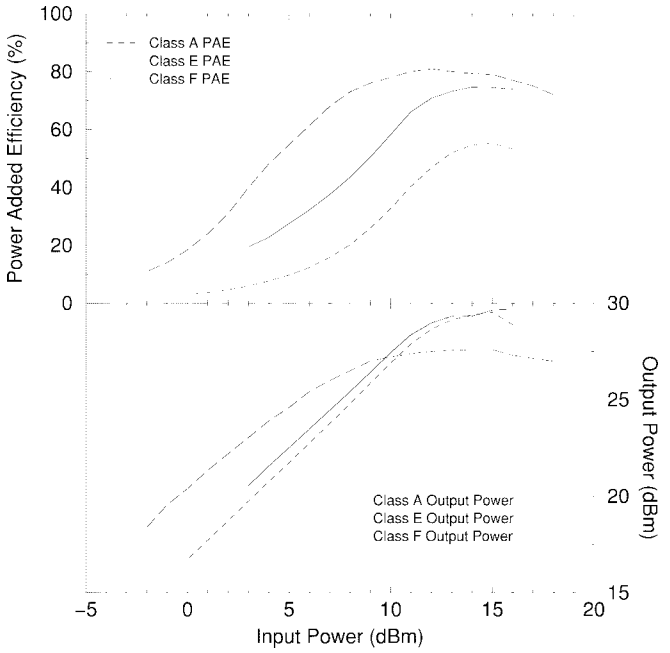

Fig. 3. Output power and PAE power sweeps for the 500-MHz Siemens CLY5 class-A ($V_{\rm DS} = 5$ V, $I_{\rm DS} = 318$ mA), class-E ($V_{\rm DS} = 6$ V, $I_{\rm DS} = 111$ mA), and class-F ($V_{\rm DS} = 6$ V, $I_{\rm DS} = 196$ mA) amplifiers.

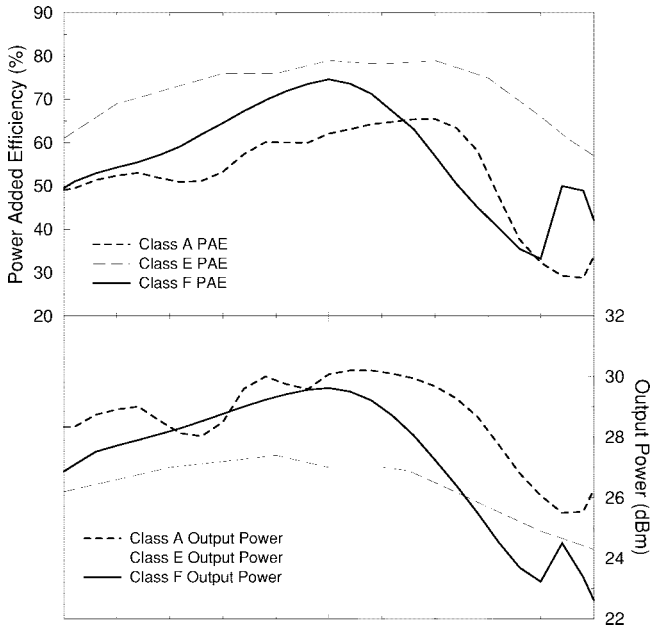

Fig. 4. Output power and PAE frequency sweeps for the 500-MHz Siemens CLY5 class-A, class-E, and class-F amplifiers.

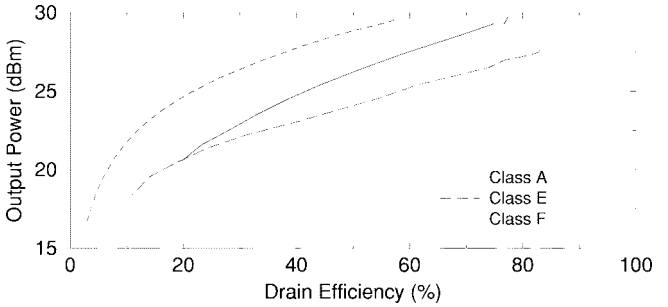

Fig. 5. Output power as a function of drain efficiency for the 500-MHz Siemens CLY5 class-A, class-E, and class-F amplifiers.

As before, a sinusoidal load current is assumed. Analysis of the lossy circuit gives an expression for dc to RF conversion efficiency, or drain efficiency (η_d); in the case of an FET,

$$\eta_d = \frac{1 + \left(\frac{\pi}{2} + \omega_s C_s R_s\right)^2}{\left(1 + \frac{\pi^2}{4}\right)(1 + \pi\omega_s C_s R_s)^2}. \tag{19}$$

This expression for drain efficiency shows that the product $\omega_s C_s R_s$ is much less than unity for a practical high-efficiency class-E circuit. Initial assumptions dictate that this expression should only be used for drain efficiencies above 60%.

III. Experimental Results

A. Comparison with Class A and Class F

In [12], three experimental class-E circuits are presented using the Siemens CLY5 MESFET at 0.5, 1, and 2 GHz. To compare the class-E amplifier with other topologies, a class-A and switched-mode class-F amplifier are designed and built at 500 MHz using the same transistor and substrate as the class-E amplifier. The class-A and class-F amplifiers are designed using the values for C_s and L_s obtained when designing the class-E amplifier. The class-F amplifier is designed to present a short to the switch at the second harmonic. The fundamental is matched for maximum power delivered to the load.

The output power and PAE are measured as a function of input power level and frequency for both the class-A and class-F amplifiers and plotted together with the results for the 500-MHz class-E amplifier. The power sweep is plotted in Fig. 3, and the frequency sweep is plotted in Fig. 4. As the device is driven into saturation, the class-A amplifier is no longer class-A, but class-AB. It is interesting to note that the gain of the class-E amplifier compresses at a lower input power level than the gain of the class-F. This is because the second harmonic short in the class-F flattens the switch-voltage waveform, reducing the peak stresses on the transistor.

While the class-E amplifier yields the highest efficiency, Fig. 5 shows that, for a given efficiency, the class-F amplifier generates more output power.

B. Two Microstrip 5-GHz Class-E Power Amplifiers

For a higher frequency class-E power amplifier, two packaged MESFET's are considered: the Fujitsu FLK052WG and FLK202MH-14. Both of these devices are designed for *Ku*-band (12–15 GHz) power amplification. At these frequencies, these MESFET's operate at approximately 30% PAE. Using these devices at a lower frequency, i.e., 5 GHz, allows for the harmonic waveshaping required for class-E operation, analogous to using the 2.5 GHz CLY5 at 0.5 and 1 GHz.

For an initial design of the two class-E amplifiers, the output capacitance and inductance C_s and L_s of the devices are estimated using S-parameters given in the data sheets and knowledge of the expected approximate output power

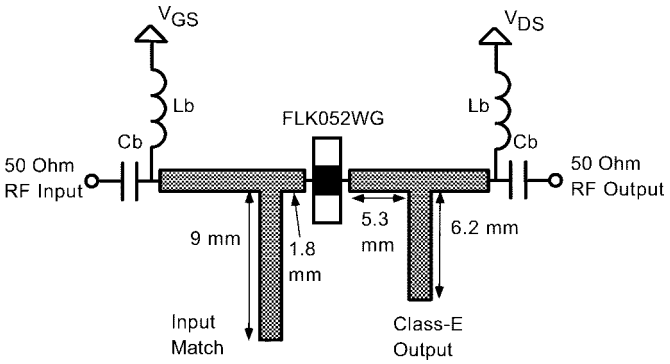

Fig. 6. The FLK052WG class-E microstrip power amplifier. This amplifier delivers 0.61 W into 50 Ω, with a compressed gain of 9.8 dB, a drain efficiency of 81%, and a PAE of 72% at 5.0 GHz. The substrate is Duroid with $\epsilon_r = 2.2$, $h = 0.508$ mm, and all lines are 50 Ω (1.6-mm wide).

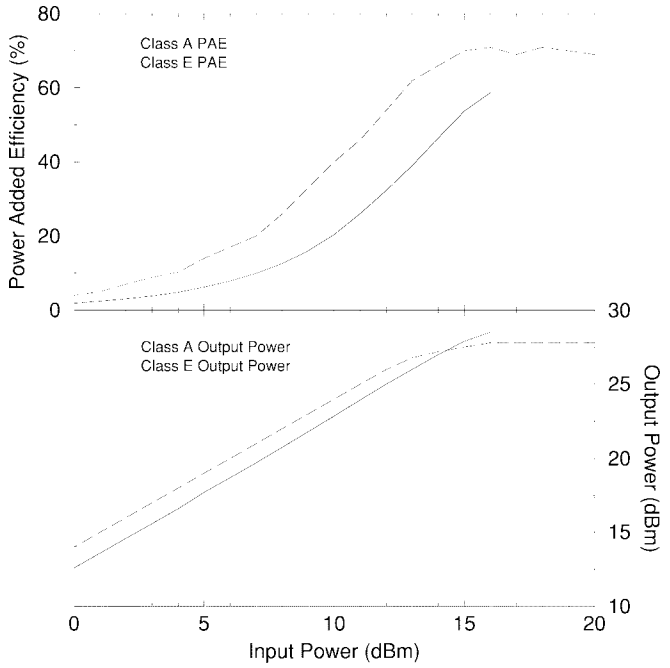

Fig. 7. Power sweep for the FLK052WG class-A ($V_{\rm DS} = 8$ V, $I_{\rm DS} = 128$ mA) and class-E ($V_{\rm DS} = 8$ V, $I_{\rm DS} = 93$ mA) amplifiers. Output power and PAE are plotted as a function of input power level.

of the amplifiers at 5 GHz. The output power of the class-E amplifier is proportional to the capacitance across the switch in the circuit (C_s). Equation (11) is then used to design the output matching circuit. S-parameters are also used to design a single-stub input-matching circuit for the two devices. These dimensions are used as a starting point for the experimental circuits, then the dimensions are experimentally adjusted until maximum PAE is obtained. The bias point and input power levels are also experimentally adjusted. The topology of these two class-E amplifiers is the same as the topology used for the amplifiers in [12], as shown in Fig. 6.

The FLK052WG class-E amplifier demonstrates an output power of 0.61 W, compressed gain of 9.8 dB, drain efficiency of 81%, and PAE of 72% at 5 GHz. The input power is 18 dBm (63 mW). The FLK202MH-14 class-E amplifier demonstrates an output power of 1.8 W, compressed gain of 7.6 dB, drain efficiency of 73%, and PAE of 60% at 5.1 GHz. The input power is 25 dBm (316 mW). Although the FLK202MH-14

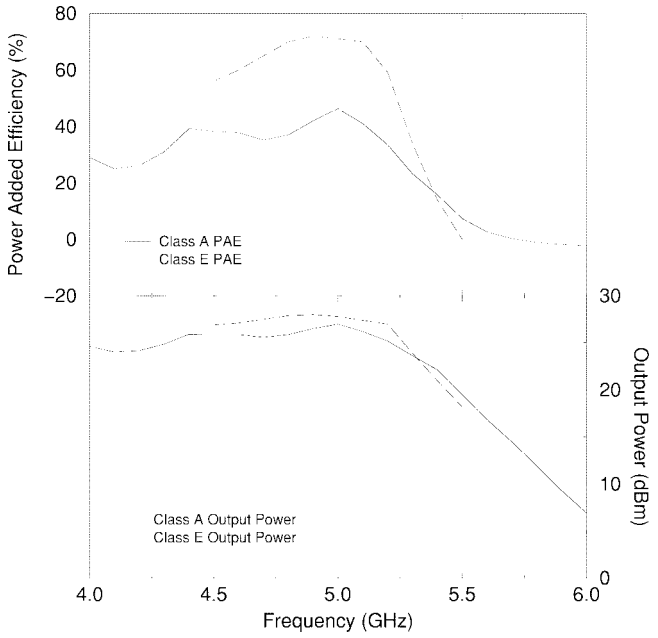

Fig. 8. Frequency sweep for the FLK052WG class-A and class-E amplifiers. Output power and PAE are plotted as a function of frequency of operation.

TABLE I
SIMULATED AND MEASURED VALUES FOR PAE AND OUTPUT POWER. A MATERKA–KACPRZAK NONLINEAR TRANSISTOR MODEL IS USED IN THE SIMULATIONS

f	$\mathbf{PAE_S}$	$\mathbf{PAE_M}$	$\mathbf{Power_S}$	$\mathbf{Power_M}$
0.5GHz	78.49%	80%	27.8dBm	27.4dBm
1GHz	72.49%	73%	30dBm	29.73dBm
2GHz	51.37%	54%	29.13dBm	27.24dBm

amplifier delivers a higher output power into 50 Ω, it operates at a lower efficiency, and it requires five times as much input power to operate in class-E mode.

The output power and PAE are measured as a function of the input power level and frequency for the FLK052WG class-E amplifier. The results are plotted together with a class-A power amplifier using the same device. The power sweep is plotted in Fig. 7, and the frequency sweep is plotted in Fig. 8. The PAE is greater than 70% over a 5% bandwidth and greater than 60% over a 10% bandwidth.

IV. HARMONIC-BALANCE CIRCUIT SIMULATIONS

In order to verify that the fabricated circuits operate in class-E mode, five-tone harmonic-balance analysis is used to simulate the circuits with Compact Software's Harmonica.[1] A Materka–Kacprzak model [16] for the Siemens CLY5 MESFET supplied by Compact Software is used for the simulations.

Experimentally obtained amplifier circuits at 0.5, 1, and 2 GHz are simulated, and the results are presented in Table I. Simulated current and voltage waveforms of the transistor have the characteristic shape of the ideal class-E circuit, as shown in Fig. 9. The discrepancies in efficiency and power simulations are larger for higher levels of saturation. We feel that the nonlinear models need to be improved for heavily

[1] *Microwave Harmonica PC*, Version 6.0, Compact Software Inc., Patterson, NJ.

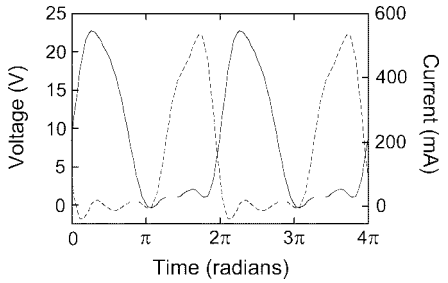

Fig. 9. Simulated voltage (solid line) and current (dashed line) waveforms at 500 MHz using the Materka model for the Siemens CLY5 MESFET.

saturated transistors. Unfortunately, a good nonlinear model is not available for the FLK052 MESFET, so no simulations are presented for amplifiers using this device.

V. A Free-Space Class-E Amplifier Array

In this section, a high-efficiency active-antenna array, which amplifies a plane wave in transmission, is presented. Such arrays can be used for large-scale power combining [17]. In the active array presented here, a plane wave is incident on an array of antennas, each one connected to an amplifier input. The outputs of the amplifiers are each connected to an output antenna. The array of output antennas radiates an amplified plane wave [18]. If all of the amplifiers are in phase, their output powers are added in free space. It is also possible to focus the wave at the input and/or output in a lens amplifier, such as the one demonstrated in [18]. Since the active elements are integrated within each input/output antenna pair, there is no feed circuitry. This reduces the size, complexity, loss, and dispersion, as compared to standard antenna arrays. Due to the transmission-mode operation of these two-dimensional arrays, traditional heat sinks cannot be used. Therefore, efficiency is a prime concern, and it is addressed by integrating appropriate antenna elements with the class-E amplifiers described in Section III. A 4-element active-antenna array is shown in Fig. 10. The amplifier circuits are microstrip, and the antennas are antiresonant slot antennas in the microstrip ground plane coupled to the microstrip feed lines.

A. The Antiresonant Slot Antenna and Bias Network

An antiresonant slot antenna is chosen as the array radiating element. This type of antenna is broad-band and can be designed to have a 50-Ω input impedance, as shown in [18]. Each of the antennas in the array are fed by a open microstrip line, which extends about a guided quarter-wavelength ($\lambda_g/4$) beyond the center of the slot. The open circuit is transformed to a short at the plane of the slot. A single antenna is measured to have a 2:1 voltage standing-wave ratio (VSWR) bandwidth of 20% with a cross-polarization ratio of 23 dB at a center frequency of 5 GHz.

B. High-Efficiency-Amplifier Array Design and Measurements

In an active-antenna array, it is important to provide bias lines which do not affect the stability of the amplifier. As shown in Fig. 10, high-impedance bias lines are connected to the voltage nulls along the gate and drain circuit stubs. The

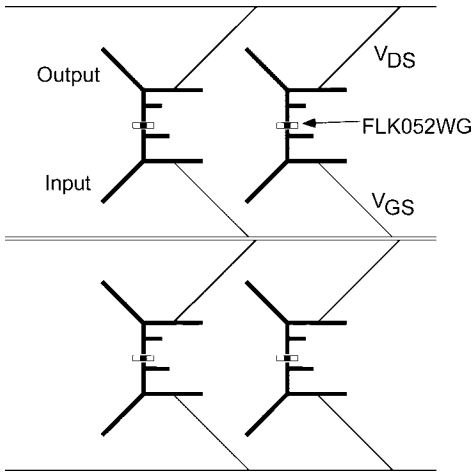

Fig. 10. The class-E power-amplifier antenna array. This four-element power-combining structure demonstrates 2.4 W of output power at 5.05 GHz, with 8.8-dB compressed gain, 74% drain efficiency, and 64% PAE. Antiresonant 50-Ω orthogonally polarized slot antennas couple the power between the amplifier and free space, while half-wave microstrip lines provide bias to the Fujitsu FLK052WGs' gate and drain terminals.

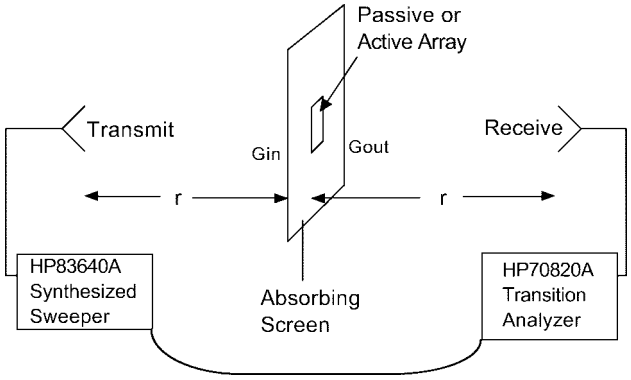

Fig. 11. Measurement setup for the 5-GHz class-E power-amplifier array. First, a passive structure is placed into the system (with 50-Ω lines connecting the input and output antennas), and a calibration power level is measured. The amplifier array is then placed in the system, and the gain and power levels are determined.

amplifiers are the same as the Class-E amplifiers described in Section III. Both the input and output loads are now the antennas, which are frequency-dependent impedances equal to 50-Ω only at the fundamental 5-GHz frequency. The impedance of the slot antennas is unimportant at the second harmonic, since the open-circuit condition satisfied by the class-E circuit is not load-dependent. The input and output slot arrays are orthogonally polarized to provide input/output isolation and stability.

The free-space measurement setup is shown in Fig. 11. An absorbing aperture is placed halfway between two horn antennas and in the far field of both antennas. The Friis transmission formula can be applied to this setup two times from one horn to the other, and the amplifier gain can be calculated if the input and output passive antenna array gains are known [18]. For calibration, a passive array similar to the one from Fig. 10, but with 50-Ω through lines instead of the amplifiers, is placed in the absorbing aperture. This calibration allows us to calculate the effect of the antennas on the power received at the second horn relative to the power transmitted from the first horn. When the amplifier is placed

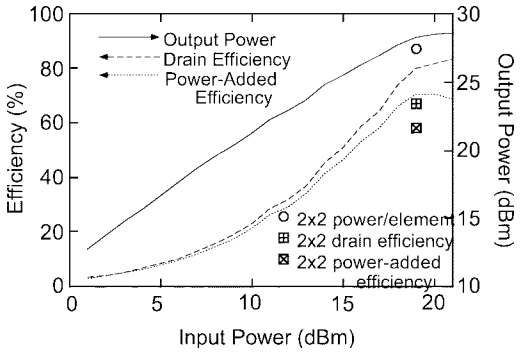

Fig. 12. Power sweep for the single-cell class-E power-amplifier element. Output power, drain efficiency, and PAE are plotted as a function of the input power level. The results of the 2 × 2 amplifier array are superimposed on the graph; the output power in this case is plotted *per element*.

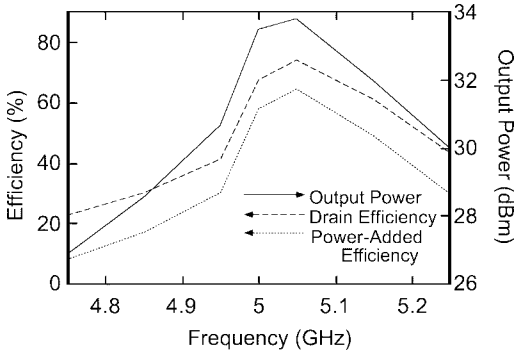

Fig. 13. Frequency sweep for the 2 × 2 class-E power-amplifier array. Output power, drain efficiency, and PAE are plotted as a function of operating frequency. The input power level is +25 dBm at 5 GHz.

in the aperture, 10 W of power is required at the transmitter to saturate the amplifier with about 320 mW incident on the array in the far field. The array radiates a maximum of 2.4 W at 5.05 GHz with 74% drain efficiency, 64% PAE, and a compressed gain of 8.8 dB contributed by the transistors.

It is interesting to examine the power-combining efficiency of the array. At the design frequency of 5 GHz, a single element of the array radiates 0.67 W with a drain efficiency of 80%, PAE of 71%, and a compressed gain of 9.3 dB. The entire array gives 2.24 W at 5 GHz, which means that the power-combining efficiency is 84%. This is illustrated in Fig. 12, which shows the power sweep of the single element with superimposed values for the array output power per element at 18-dBm input power. The measured frequency dependence of the output power, drain efficiency, and PAE is shown in Fig. 13.

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